ADF5611/ADF5612 Data Sheet Revision

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Table 1. Specifications

FROM Rev 0

PDIV_OUT and NDIV_OUT Power	P_{O_DIV}	3	dBm	Single-ended, DIV_PWR = 3
		6	dBm	Differential, DIV_PWR = 3

TO Rev 1

Add footnote :

DIV_PWR setting 1 and 2 have the same output power levels.

Table 15. Manually Programmed VCO Calibration Settings

FROM Rev 0

Table 15. Manually Programmed VCO Calibration Settings

Bit Fields	Value	Description
O_VCO_DB	0x1	Manually calibrated values are double buffered by programming N_INT.
EN_AUTOCAL	0x0	Disables autocalibration.
EN_DNCLK	0x0	Disables DIV_NCLK to the digital block.
EN_ADC_CLK	0x0	Disables the ADC clock.
O_VCO_CORE	0x1	Overrides the VCO core with value in M_VCO_CORE.
O_VCO_BAND	0x1	Overrides the VCO band with M_VCO_BAND.
O_VCO_BIAS	0x1	Overrides the VCO bias with M_VCO_BIAS.
M_VCO_CORE	Program with recorded values	Selects the VCO core when O_VCO_CORE = 1.
M_VCO_BAND	Program with recorded values	Selects the band within the core when O_VCO_BAND = 1.
M_VCO_BIAS	Program with recorded values	Selects the bias value used when O_VCO_BIAS = 1.
Configure Target Frequency Parameters	Program RFOUT	Sets the corresponding N_INT, FRAC1WORD, FRAC2WORD, and MOD2WORD. Ensure that Register 0x10 is the last write command.

TO Rev 1

Table 15. Manually Programmed VCO Calibration Settings

Bit Fields	Value	Description
O_VCO_DB	0x1	Manually calibrated values are double buffered by programming N_INT.
EN_AUTOCAL	0x0	Disables autocalibration.
EN_DNCLK	0x0	Disables DIV_NCLK to the digital block.
EN_ADC_CLK	0x0	Disables the ADC clock.
O_VCO_CORE	0x1	Overrides the VCO core with value in M_VCO_CORE.
O_VCO_BAND	0x1	Overrides the VCO band with M_VCO_BAND.
O_VCO_BIAS	0x1	Overrides the VCO bias with M_VCO_BIAS.
M_VCO_CORE	Program with recorded values	Selects the VCO core when O_VCO_CORE = 1.
M_VCO_BAND	Program with recorded values	Selects the band within the core when O_VCO_BAND = 1.
M_VCO_BIAS	Program with recorded values	Selects the bias value used when O_VCO_BIAS = 1.
Configure Target Frequency Parameters	Program RFOUT	Sets the corresponding N_INT, FRAC1WORD, FRAC2WORD, and MOD2WORD. Ensure that Register 0x10 is the last write command.
RST_SDM	0x1 followed by 0x0	Reset SDM Block. Set to 1 and then to 0 when going from an integer to fractional frequency or fractional to integer frequency.

Table 16. ADF5611 Register Map

FROM Rev 0

0x029	LDWIN_PW				LD_COUNT				0x00	R/W
0x02A	0	1	EN_LOL	EN_LDWIN	RESERVED	RST_LD	ABPW_WD	RESERVED	0x00	R/W
0x02B	MUXOUT				EN_MUXOUT	EN_CPTEST	CP_DOWN	CP_UP	0x04	R/W

0x03E	RESERVED								0x00	R/W
0x03F	0	1	0	1	0	1	0	0	0x00	R/W
0x040	RESERVED		1	0	1	0	1	1	0x00	R/W

TO Rev 1

0x029	LDWIN_PW				LD_COUNT				0x00	R/W
0x02A	0	1	EN_LOL	EN_LDWIN	RESERVED	RST_LD	ABPW_WD	RST_SDM	0x00	R/W
0x02B	MUXOUT				EN_MUXOUT	EN_CPTEST	CP_DOWN	CP_UP	0x04	R/W

0x03E	RESERVED								0x00	R/W
0x03F	0	1	0	1	1	1	0	1	0x00	R/W
0x040	RESERVED		1	0	1	0	1	1	0x00	R/W

Table 59. Bit Descriptions for REG002A

FROM Rev 0

Table 59. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	REG2A_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG2A_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	EN_LOL	Enables loss of lock detector. 0: disables loss of lock detector. 1: enables loss of lock detector.	0x0	R/W
4	EN_LDWIN	Enables the lock detector pulse window. 0: lock detector pulse window disabled. 1: lock detector pulse window enabled.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	RST_LD	Resets the lock detector to the unlocked state. 0: resets to inactive. 1: resets to active.	0x0	R/W
1	ABPW_WD	PFD Antibacklash Pulse Width.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

TO Rev 1

Table 59. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	REG2A_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG2A_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	EN_LOL	Enables loss of lock detector. 0: disables loss of lock detector. 1: enables loss of lock detector.	0x0	R/W
4	EN_LDWIN	Enables the lock detector pulse window. 0: lock detector pulse window disabled. 1: lock detector pulse window enabled.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	RST_LD	Resets the lock detector to the unlocked state. 0: resets to inactive. 1: resets to active.	0x0	R/W
1	ABPW_WD	PFD Antibacklash Pulse Width.	0x0	R/W
0	RST_SDM	0: Reset SDM Disabled. 1: Reset SDM Enabled.	0x0	R/W